NOTRE DAME UNIVERSITY BANGLADESH

VLSI Design Lab Report-04

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Course Title: VLSI Design Lab
Experiment Name: Implementing FlioFlop Circuit

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Abstract

This laboratory experiment presents the design and CMOS implementation of a flip-flop circuit using the DSCH2 schematic simulation tool. A D Flip-Flop was realized using CMOS logic principles and its functional behavior was verified through truth table analysis and timing simulation. The circuit operation was analyzed with respect to clock-triggered input transitions, and the timing diagram was used to observe the synchronization between input and output signals. The experimental results confirm that the implemented flip-flop exhibits correct edge-triggered behavior and maintains stable data storage, consistent with theoretical expectations.

1 Introduction

This laboratory experiment focuses on the design and implementation of a flip-flop circuit using CMOS logic in the DSCH2 environment. Flip-flops are fundamental sequential elements used for data storage and synchronization in digital systems. In this experiment, a D Flip-Flop was designed using CMOS-based logic gates, and its functionality was verified through truth table analysis and timing simulation. The behavior of the circuit was observed with respect to clock-triggered input transitions.

2 Objective

The objectives of this laboratory experiment are as follows:

- To design and implement a flip-flop circuit using CMOS logic.
- To develop schematic-level circuits using the DSCH2 tool.
- To derive and verify the truth table of the flip-flop from simulation.
- To analyze timing diagrams to observe clock-triggered behavior.
- To understand the operation of sequential circuits and data storage elements.

3 Function

The D Flip-Flop is a clock-controlled bistable device that transfers the input data (D) to the output (Q) on the active edge of the clock signal.

$$Q_{next} = D$$

The output changes only at the triggering edge of the clock, ensuring synchronized data storage.

Truth Table

Clock	D	Q(next)
↑	0	0
↑	1	1
No Edge	X	Q(previous)

Schematic Image

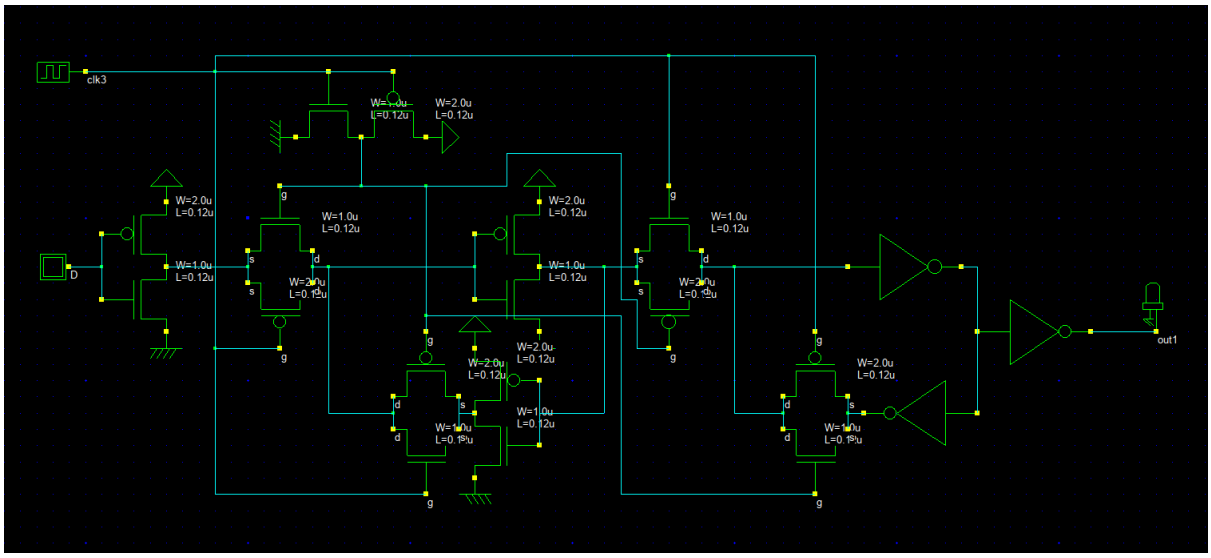

Figure 1: CMOS Schematic of D Flip-Flop in DSCH2

Timing Diagram

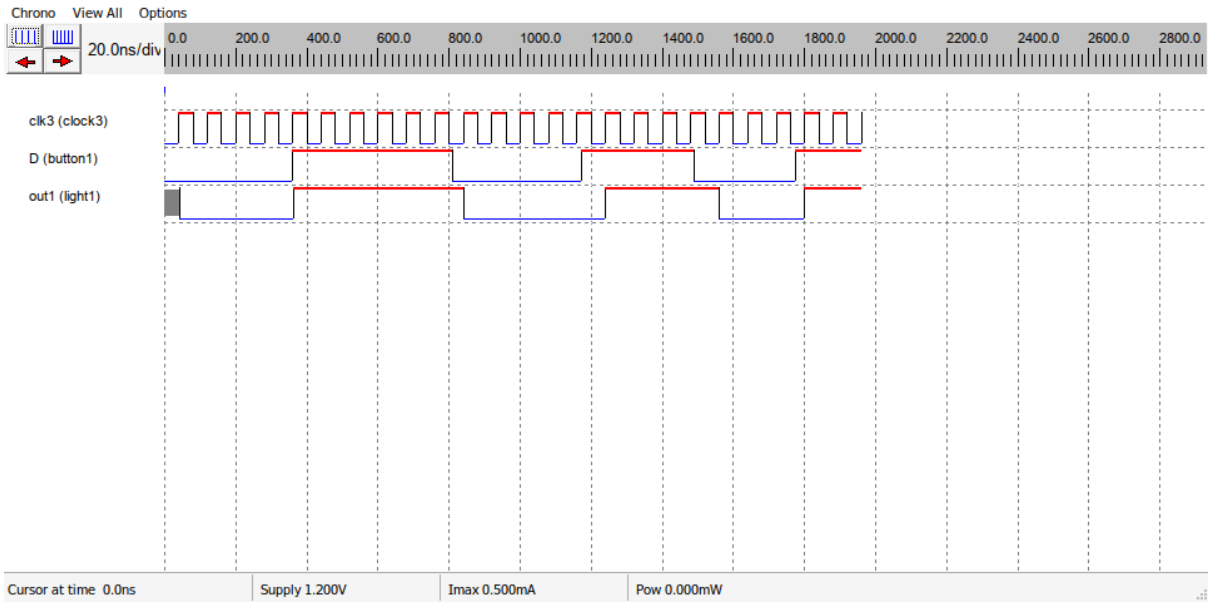

Figure 2: Timing Diagram of D Flip-Flop

The timing diagram shows that the output Q follows the input D only at the rising edge of the clock signal. Between clock edges, the output remains constant regardless of changes in the input.
From the simulation results, it was observed that the D Flip-Flop changes its output state only at the rising edge of the clock signal. When the clock transitions from LOW to HIGH, the output Q takes the value of the input D. At all other times, the output remains unchanged, preserving the previously stored value. This behavior confirms the correct operation of the edge-triggered D Flip-Flop implemented using CMOS logic.

4 Conclusion

The CMOS-based D Flip-Flop was successfully designed and simulated using the DSCH2 tool. The truth table and timing diagram verified that the circuit operates correctly as a clocked storage element. This experiment reinforces the understanding of sequential logic design and the role of flip-flops in digital systems.